

FIG. 1

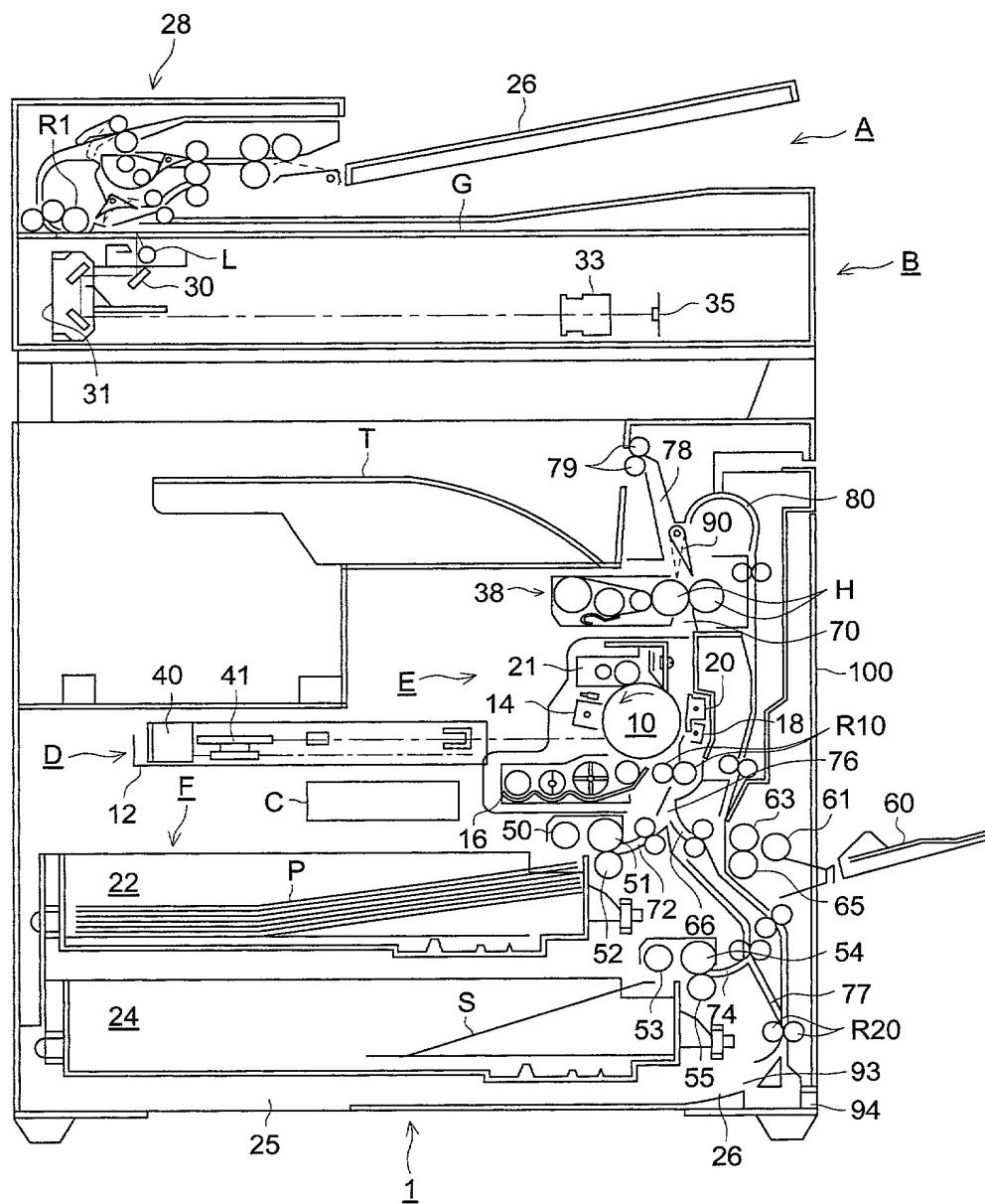
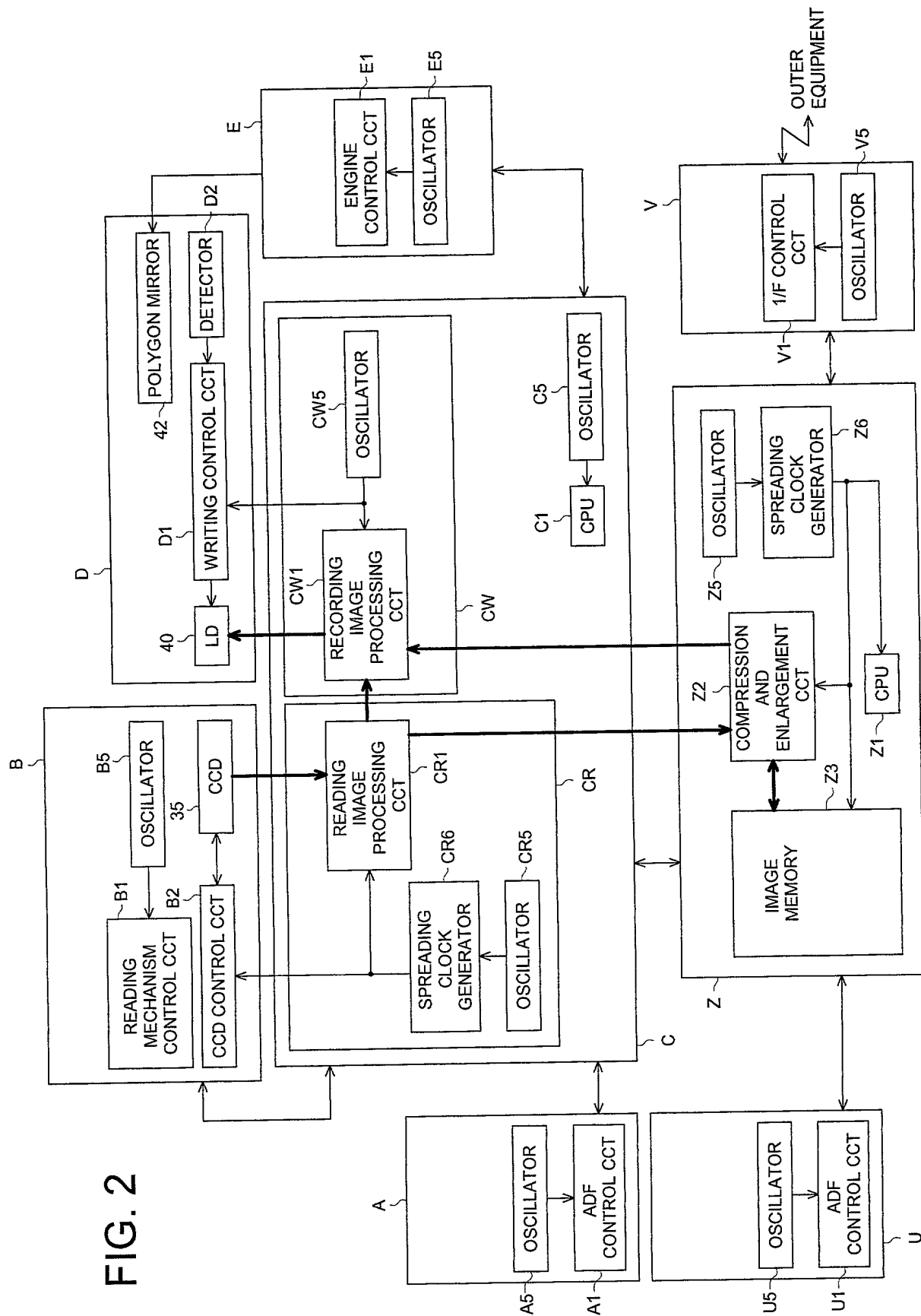


FIG. 2



The graph shows Frequency on the vertical axis and Time on the horizontal axis. A solid line represents a periodic triangular waveform. A dashed line represents the envelope of the signal, which is also periodic and triangular. The period of the signal is labeled T . The frequency of the signal is labeled N_r .

FIG. 4

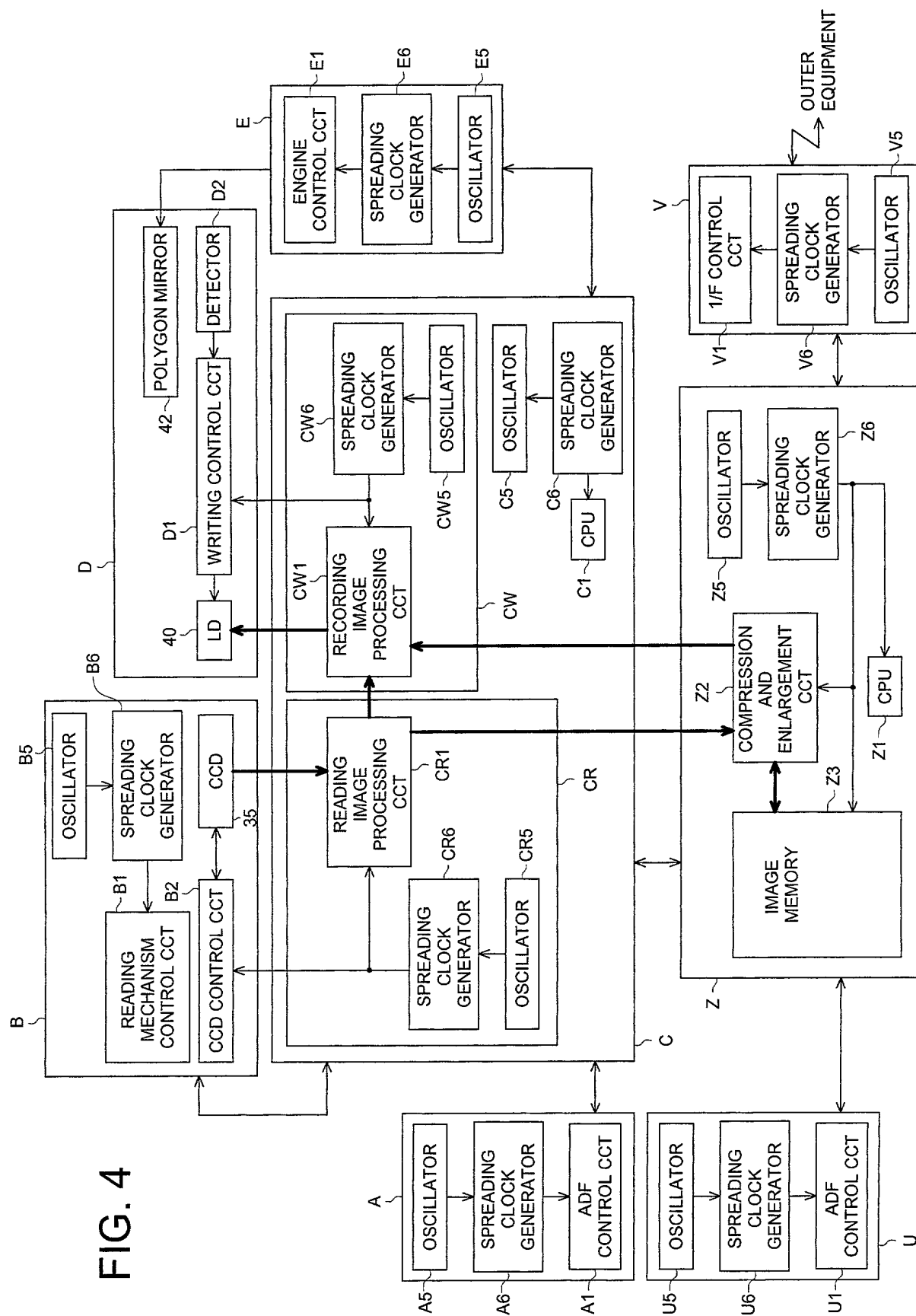


FIG. 5

The diagram illustrates a video recording and reproduction system, labeled FIG. 5. The system is organized into several main functional blocks, each containing sub-components and interconnected by control and data lines.

- Block A (ADF Control CCT):** Contains an OSCILLATOR (A5), a SPREADING CLOCK GENERATOR (A6), and an ADF CONTROL CCT (A1).
- Block B (Reading Mechanism Control CCT):** Contains a READING MECHANISM CONTROL CCT (B1), a CCD CONTROL CCT (B2), an OSCILLATOR (B5), a SPREADING CLOCK GENERATOR (B6), and a CCD (35).
- Block C (Image Processing CCT):** Contains a READING IMAGE PROCESSING CCT (CR1), a SPREADING CLOCK GENERATOR (CR6), an OSCILLATOR (CR5), and a TEMPORARY MEMORY SECTION. It is connected to Block B and Block D.
- Block D (Writing Control CCT):** Contains an LD (40), a WRITING CONTROL CCT (D1), a POLYGON MIRROR (42), a DETECTOR, and a TEMPORARY MEMORY SECTION. It is connected to Block C and Block E.
- Block E (Engine Control CCT):** Contains an ENGINE CONTROL CCT (E1), a SPREADING CLOCK GENERATOR (E6), an OSCILLATOR (E5), and a TEMPORARY MEMORY SECTION. It is connected to Block D.
- Block V (1/F Control CCT):** Contains a 1/F CONTROL CCT (V1), a SPREADING CLOCK GENERATOR (V6), an OSCILLATOR (V5), and a TEMPORARY MEMORY SECTION. It is connected to Block E.
- Block Z (Image Memory and Compression):** Contains an IMAGE MEMORY, a COMPRESSION AND ENLARGEMENT CCT (Z2), a CPU (Z1), an OSCILLATOR (Z5), a SPREADING CLOCK GENERATOR (Z6), and a TEMPORARY MEMORY SECTION. It is connected to Block C and Block V.

The system also includes a CPU (C1) and a TEMPORARY MEMORY SECTION (C6) within Block C. The diagram shows the flow of data and control signals between these components, including the use of temporary memory sections for data storage and retrieval.

FIG. 6

